Reliability and Characteristics for Wafer Level Chip Scale Packages under Current Stressing

Po-Ying Chen[1], Heng-Yu Kung[2, 3], Yi-Shao Lai[3], Ming Hsiung Tsai[1], and Wen-Kuan Yeh[2]

[1] Department of Information Engineering, I-Shou University, NO.1, Sec. 1, Syuecheng Rd., Dashu Township, Kaohsiung county, 840 , Taiwan (R.O.C.)

[2] Department of Electronic Engineering, National University of Kaohsiung, No. 700, Kaohsiung University Road., Nan-Tzu Dist., Kaohsiung 811, Taiwan, R.O.C.

[3] Stress-Reliability Lab, Advanced Semiconductor Engineering, Inc. Taiwan, R.O.C.

Tel: 886-7-6577711 ext 3394, Fax: 886-7-6577056, E-mail: PLin121@ms.ccafps.khc.edu.tw

Abstract

This work presents a novel approach and method for examining the characteristics of wafer-level chip-scale packages (WLCSPs) for electro migration (EM) tests. The die in the WLCSP was directly attached to the substrate via a soldered interconnect. The die shrinks area available for power and the solder bump also shrinks volume and increase quantity of electron for interconnect efficiency. The bump current density now approaches 10^6 A/cm^2, at which point the electromigration (EM) becomes a significant reliability issue. As known, the EM failure depends on numerous factors, including the working temperature and the under bump metallization (UBM) thickness and others.

New interconnection geometry has been used utilized extensively with moderate success in overcoming larger mismatches in components displacements during current and temperature excursions. Both the environments and testing qualifications for these packages are becoming increasingly more and more demanding. Failure mechanisms once considered eliminated, or at least reduced to a manageable

extent in new package technology designs, are again challenging process integrity and reliability. Especially for WLCSPs, which were first designed to eliminate any need for encapsulation to be compatible with the smart-mount technology (SMT) process, and to have good handing properties face serious reliability problems?

This study investigated the reliability of a WLCSP subjected to different accelerated current stressing conditions at a fixed ambient temperature of 125°C. A reasonably strong correlation existed between mean-time-to-failure (MTTF) of the WLCSP test vehicle and the average current density carried by a solder joint was obtained.

A series of current densities were also applied on to WLCSP architecture; Black's power law was utilized to simulate for the failure mode analysis. Furthermore, SEM was implemented to determine which levels differences were existed between high and low current density failure modes.

KEYWORDS: Wafer Level Chip Scale Package, Mean-time-to-failure (MTTF), Current Stressing, Smart mount technology (SMT), Reliability.

I. Introduction:

Semiconductor reliability is continuously improving. The wafer level chip scale package (WL-CSP) was recently developed under various demands- small outline, lightweight, high input and output (I/O) density, and good electrical performance- for mobile consumer electronic devices such as cellular phones, pagers, and personal digital assistant (PDAs). Generally, WLCSPs, which were first designed to eliminate the need for encapsulation, to be SMT-processes compatible, and to have good handling properties, now face some reliability problems.

The trend in the ultra large scale integrity circuit (ULSI) technology has resulted in excessively narrow interconnection lines and small contact area[1]. These characteristics have aggravated the electromigration-induced failure problems which are particularly critical for WLCSPs. To achieve design in reliability, one must be able to determinate the maximum current density guidelines in the conductors and at contact point and be able to efficiently evaluate and correct potential EM failures during the circuit design phase[2,3].

As integrated circuit (IC) technology continues to advance, will increase demands on I/O counts and power requirements, resulting in decreased solder pitch and increased current density for solder balls in high-density chip-scale packages (CSPs). Consequently, WLCSPs were developed to have smaller geometry, lighter, higher density and better electrical performance than existing traditional package. With the growing proliferation of WLCSPs, target applications are increasingly focused on hand-held devices and consumer applications such as in cellular phones, pagers, and PDA's etc.

Thus, as bump sizes continue to decrease, analysis of EM reliability becomes crucial in order to understanding and preventing failure causes. Identifying the reliability of WLCSPs under current stress has

become a crucial topic associated with reliable product design.

As the electronics industry continues to push for miniaturization, the reliability becomes a vital issue particularly as the demand for small solder bumps and increased current has resulted in a significant increase in current density[2, 3)]. Increased current densities engender concerns regarding interconnect reliability. Electromigration is a common cause of interconnect failure. In this work, EM mean time to failure (MTTF) was modeled as a function of various DC current densities.

Electromigration of CSP architecture is a relatively new field of investigation. Such investigations, require analysis of current distribution in a CSP joint configuration, due to the direct link between the atomic flux of interconnects. "Jem", and the current density, "J", in EM as derived by[4,5)]:

$$Jem = C \left(\frac{D}{kT}\right) (Z e) \rho J \qquad (1)$$

where C is a constant of atomic concentration, D is the atomic diffusion, k is the Boltzman constant, T is the absolute temperature, Z is the effective charge number, e is the electron charge, ρ is the resistivity.

Three crucial factors dominate the EM prosperities and lifetime of CSP architecture against electromigration. The first factor is the current density the second is the material diffusivity and the third is joint heat transfer in an interconnect. Diffusivity is the material property. Current density in the interconnect depends on device design. Examining or predicating failure transactions and distribution in the interconnect joint will increase understanding of CSP behavior due to EM.

II. Experimental

Figure 1 presents the equipment set up for this examination of WLCSPs' EM tests. The experiment comprises a regulated power supply, an electronic load, a heat oven, and a digital multi-meter. The heat oven is utilized for thermal aging and is maintained at $125\,^{0}C$.

The WL-CSP test vehicle was constructed by surface mounting a 6.35 mm × 6.8 mm daisy-chain chip onto a daisy-chain test board through 98 ea I/O with material of 95.5 Sn-4Ag-0.5Cu solder joints. The surface finish of board pads was electro less-plated Ni/Au. The under bump metallurgy (UBM) on the chip side was a stack of sputtered thin films of 4 kÅ Al / 3.25 kÅ Ni (V) / 8 kÅ Cu, and the trace was a stack of 2 kÅ Ti / 15 kÅ Al / 2 kÅ Ti. The pitch between adjacent solder joints was 500 um. The UBM opening was 280 um in diameter. The experimental detailed parameters were listed as Table I.

In the conventional long-term packaged EM test, relatively low current densities, ranging 0.1-0.5 MA/cm2, were used, where the Joule hating is less than only few degrees.

In the WLCSP EM test, much higher current densities were applied than in the packaged EM test, resulting in Joule heating. The Joule heating is proportional to the square of the current density[6]. Since the temperature is more critical factor than the current density in EM test, it is desirable to monitor and control temperatures then the current densities at these highly accelerated conditions. Therefore, an isothermal algorithm was used in WLCSP test, where the metal line temperature was maintained at constant by adjusting the stress period in a feedback loop during the test. Therefore, the metal line temperature was determined from the pre-measured TCR (Temperature Coefficient of Resistance) values and the resistance variation during the test.

III. Results and Discussions:

As IC patterns and devices become increasingly small, lightweight and have high working frequency, electronic packaging that applies CSP design has become preferred. The WLCSP packaging provides better signal performance than the traditional ones and can eliminate the resistance in interconnects between the chip and substrate. Furthermore, the WLCSP technology completes the packaging operation directly on the

wafer with a chip scaled size, which has a good potential for future electronic packaging. The WLCSP

structure has five components: (1) the chip, (2) UBM, (3) trace (runner), (4) solder bump, and (5) substrate.

These components are made of different materials in their architecture. It is due to the coefficient of

thermal expansion (CTE) mismatch between the silicon chip, the organic PCB, and other metal; the

reliability issues for the WLCSP with a large die size remain problematic. Figure 2(a) presents the top

surface morphology of chip packaged by WLCSP type. The solder bumps are formed directly on the pad

which defined on the surface of chip. In this study, the architecture of the WLCSP samples are described.

Figure 2 (b) presents a cross-sectional diagram of A-A' view as Fig. 2(a). Due to the CTE mismatch among

different materials in the packaging structure, this study discusses the packaging reliability under current

stressing is concerned and discussed herein. A previous study[7], determined that the solder joints in the

WLCSP are weakest because of the shear stress resulting from CTE mismatch. However, another problem

exists in that the trace cross-section area is smaller than the solder bumps shown in Figure 2(b).

It is owing to that an EM test conducted under conventional test conditions can take weeks or even

months to complete. Consequently, fast EM tests that can be conducted using a high current density and

temperature stress are becoming very popular. Although these high-stress conditions can add uncertainties

and unintended effects to the EM test, and can affect test accuracy, such testing is necessary when the test

data are to be used to predict EM performance of metal interconnects under operating conditions.

In this study, high current density stressing was utilized to analyze WLCSP properties. Figure 3 and 4

present the results of dynamic current stress using 0.5, and 0.7 Amp, respectively. Resistance was increased

after current stressing.

Since capturing accurately such a resistance leap is difficult, the mean-time-to-failure (MTTF) of the

WLCSP test vehicle was defined according to the duration over which resistance increases by 20% over initial resistance. Furthermore, this study derives *J* as the average current density by dividing applied electrical current by the area of the UBM opening. The correlation between Ln (MTTF) and Ln (J) is reasonable strong ($r^2 = 0.97$) and shown in Fig.5. Foley [8] compared normally and highly accelerated EM testing on a 5 um National Institute of Standard and Technology (NIST) metal line. Foley concluded that using a Black equation for conditions below 240 ^{o}C and current densities of 3 MA/cm^2 is safe. This power-law model is a simplified version of Black's equation, which is typically applied when characterizing the EM reliability of conductors.

The modeling of EM MTTF as a function of DC current density is well established[1,2], that is the moment of metal atoms in the current flow. The model can be described as:

$$MTTF = AW^p L^q J^{-n} \exp(E_a / kT)$$

where J is current density, Ea is activation energy, W is the width of the metal line, and L is the length of the metal line.

Electromigration is results from momentum exchange between conducting electrons and diffusing metal atoms. However, the EM characteristics of a WLCSP remain largely unknown.

Electromigration is atomic diffusion generated by a combination of high temperature and high current during which electron momentum is transferred to atoms. This phenomenon correlates with several failure mechanisms such as solder ball and silicon interface voiding caused by current crowding, and formation of inter-metallic compounds and UBM consumption generated by migrated phases.

Examining the failure mode of samples following current stress using various current densities is important. A consummation reaction of Cu occurred at the corner of a solder bump and became a second

phase grain as shown in Fig. 6. This second phase acts as a parallel resistance and increases the totals resistance. This second phase grain is always located at the interface between the bump ball and ball pad and is generally 40 um in diameter.

As mentioned above, owing to trace (runner) is to have the smallest cross-section area in the total WLCSP structure. Therefore, trace will have the largest current density loading in its architecture. The stressing current causes the runner to become thinner (Fig. 7). This phenomenon will become more critical under high current density (larger than 0.1 Amp.). Furthermore, another failure site is located near the trace. This is the first time, the second failure point has been identified and belong to high current density failure issue.

There were some voids were created at the bump ball (Fig. 8). A serious crack was occurred when the runner layer became thinner. Such cracks always located at the interface between the bump ball and runner layer and are usually about 70 um in diameter. These cracks develop very rapid and induce a rapid increase in interconnect resistance.

This study also compared the differences between samples stressed by high and low current density. Fig. 9 (a) and (b) present the morphology of scanning electron microscopy (SEM) analysis during which the samples were stressed under 0.1and 0.9 amp, respectively. These images indicate that low current density stressing induces thinning of the runner material first. The high current density stressing provides preferable results to induce crack growth. In this work, the valuable results show that different current density dominate different initiation mechanism for failure mode development. The result reveals that the redistribution traces in the WLCSP may suffer significant stress and has the possibility to form crack during high current density stressing.

Conclusions:

This study investigated the reliability of a WLCSP under accelerated current stressing conditions of 0.1, 0.5 A, 0.6 A, 0.7 A, 0.8A, and 0.9 A at a fixed ambient temperature of 125 ^{o}C.

The cross sections of solder joints were analyzed by SEM for failure mode analysis. Three failure modes were identified at the same time: (1) the solder bump, which occur copper consummation reactions, (2) the runner thins, and (3) the trace had initiated a crack occurring.

This study also compared the differences between samples stressed by high and low current density. From the SEM analysis, these images indicate that low current density stressing induces thinning of the runner material first. The high current density stressing provides preferable results to induce crack growth. The valuable results show that different current density dominate different initiation mechanism for failure mode development. The result reveals that the redistribution traces in the WLCSP may suffer significant stress and has the possibility to form crack during high current density stressing.

References

1) Lee Teck Kheng, Teo Yong Chua and Lim Thiam Beng: IEEE /CPMT Electronics Packaging Technology Conference proceeding (1998) 274.

2) S. W. Yoon, J. Ki Hong, H. J. Kim, and Kwang Yoo Byun: IEEE Transactions on electronics packaging manufacturing, **28** (2005) 168.

3) Stephen Gee , Nikhil, Joanne Huang, and King-Ning Tu: Proceeding of IPACK 2005 ASME inter Pack'05 July 17-22, San Francisco, California, USA (2005) 1-9.

4) Tien-Yu Tom Lee,Taek-Yeong Lee, and King-Ning Tu: IEEE Transactions on Components and Package Technologies, **27** (2004) No. 3, 472.

5) Huntington, H. B. and Grone, A.R: J.Phys. Chem. Solids, **20** (1961) 76.

6) W. J. Choi, E. C. C. Yeh, K. N. Tu, Journal of Applied Physics, **94** (2003) No. 9, 5665

7) D. G. Pieerce and E. S. Snyder: "Wafer Level Reliability: pushing the envelope, '' in Tutorial Notes of 35th International Reliability Physics Symposium (IRPS 97), (1997) 5.1.

8) S. Foley: Microelectronics Reliability, **38** (1998) 1021.

Figure Captions

Fig. 1. The measurement set-up of current stress experiment.

Fig. 2 The top view picture of wafer level chip scale package (WL-CSP) which were after Surface Mount

Technology (SMT) process.

Fig. 3 The results of resistance under current stressing conditions at J=0.5 Amp. and a fixed ambient

temperature of 125 $^{\circ}$C.

Fig. 4 The results of resistance under current stressing conditions at J=0.7 Amp. and a fixed ambient

temperature of 125 $^{\circ}$C.

Fig. 5 Correlation between N_f and J at a fixed ambient temperature of 125 $^{\circ}$C

Fig. 6 The failure mode analyzed by SEM at solder bump.

Fig. 7 The failure mode analyzed by SEM at runner corner.

Fig. 8 The failure mode analyzed by SEM between UBM and solder bump.

Fig. 9 The differences comparison of SEM analysis between the samples stressed by (a) 0.1 Amp and (b)

0.9 Amp. .

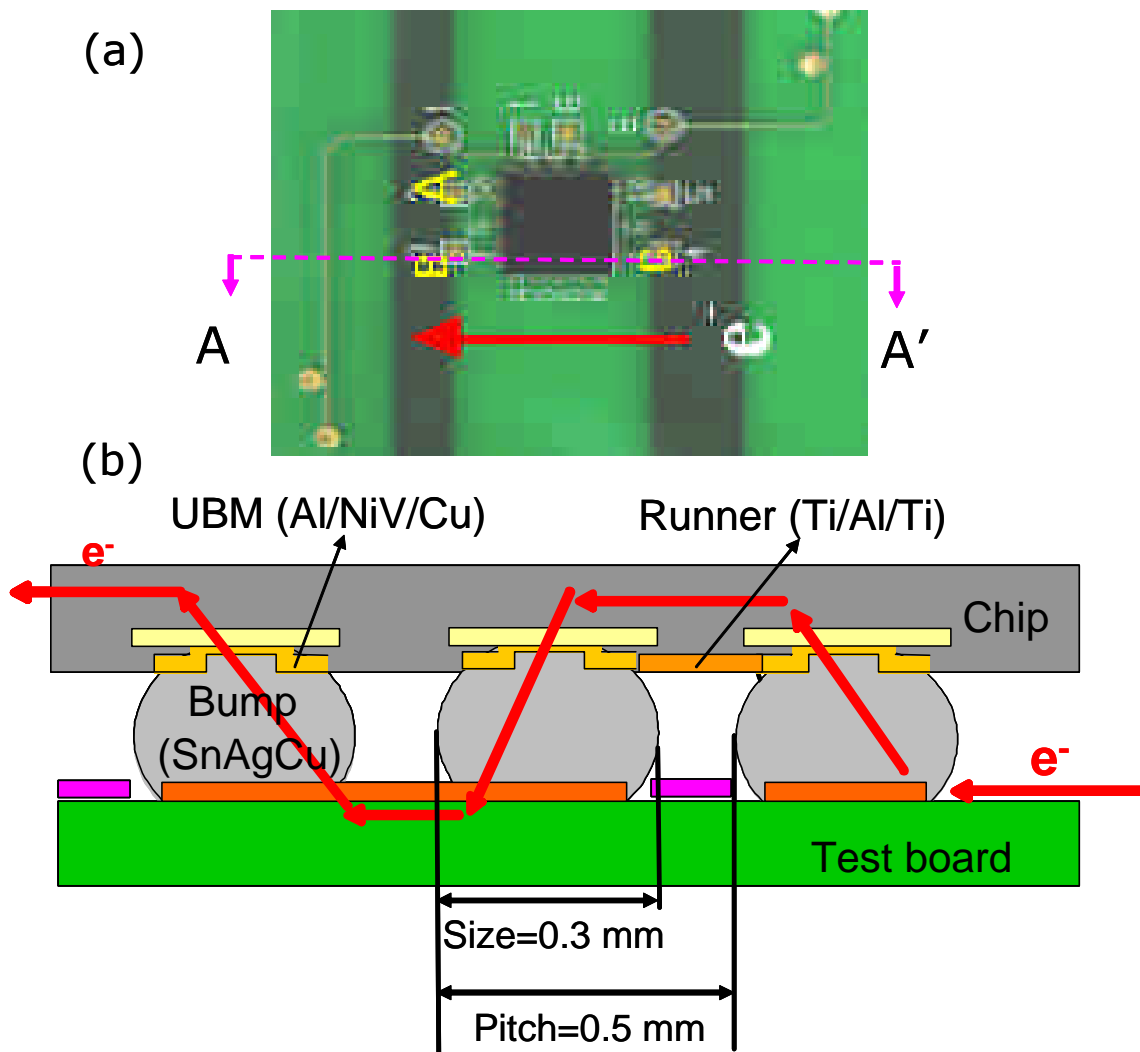Table Captions

Table I The experimental used conditions.

DC current
(From 0.5 to 0.9A)

Record
resistance

A fixed ambient
temp. : 125°C

Fig. 1

P. Y. Chen et al

(a)

A   A′

(b)

UBM (Al/NiV/Cu)   Runner (Ti/Al/Ti)

e⁻

Chip

Bump
(SnAgCu)

e⁻

Test board

Size=0.3 mm

Pitch=0.5 mm
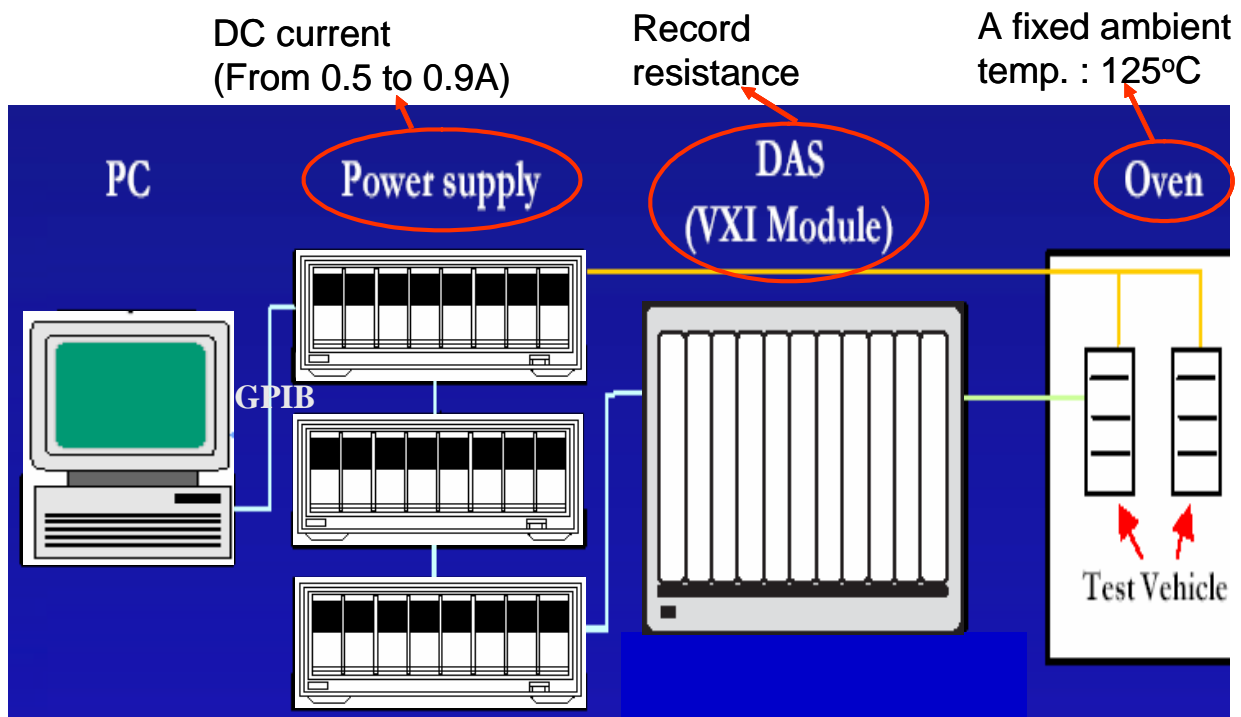
Fig. 2

P. Y. Chen et al

Current I= 0.5 Amp and T= 125 °C
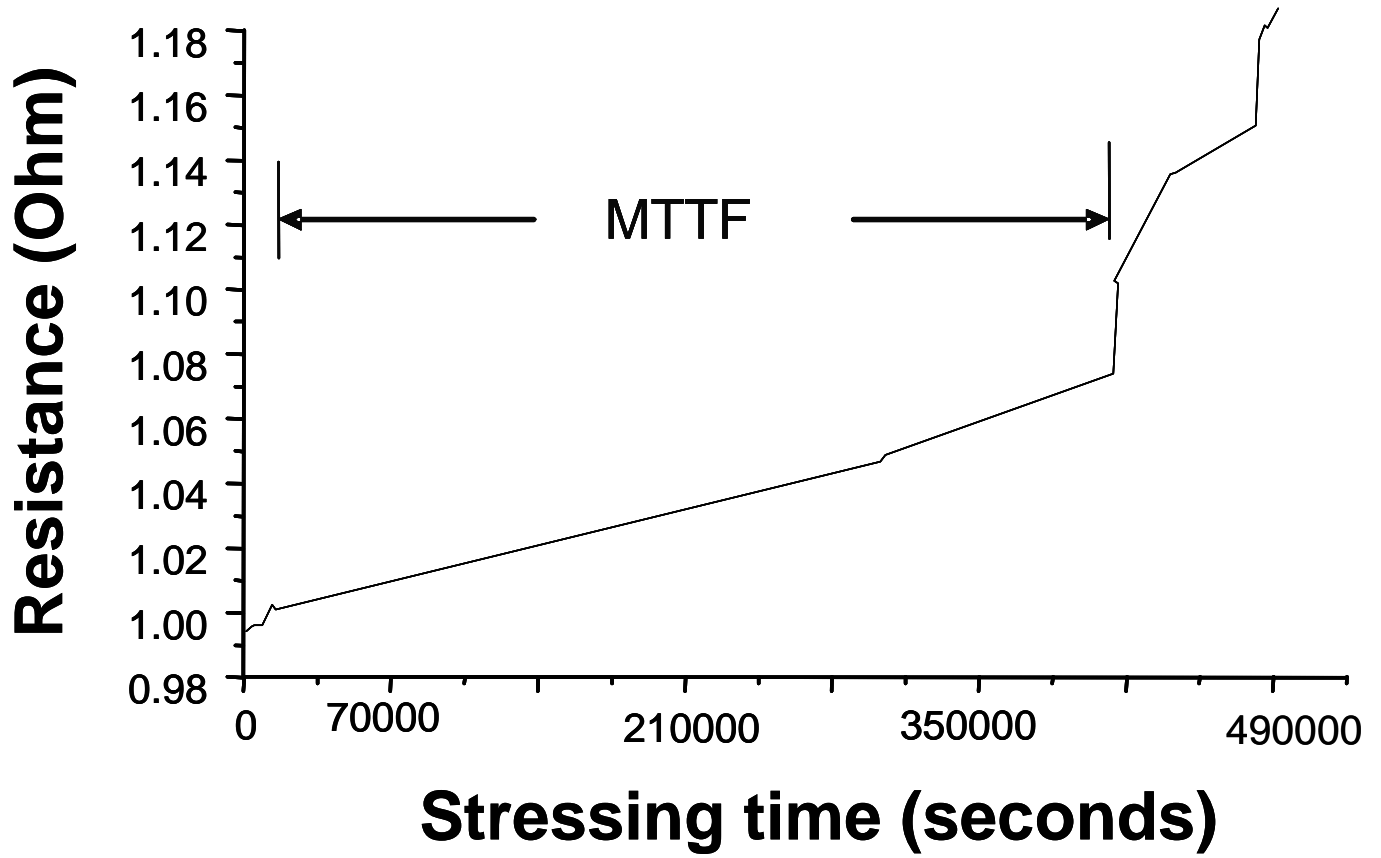
Fig. 3

P. Y. Chen et al

Current I= 0.7 Amp and T= 125 ^{o}C

Fig. 4

P. Y. Chen et al

Fig. 5

P. Y. Chen et al

Fig. 6

P. Y. Chen et al

Runner become thinner

660.00nm   1.87um

25 um

SE   10-Jan-06   R2   WD15.8mm 15.0kV x1.8k   25um

Fig. 7

P. Y. Chen et al

Crack

25 um

Fig. 8

P. Y. Chen et al

(a)

110 um

(b)

Die

50 um
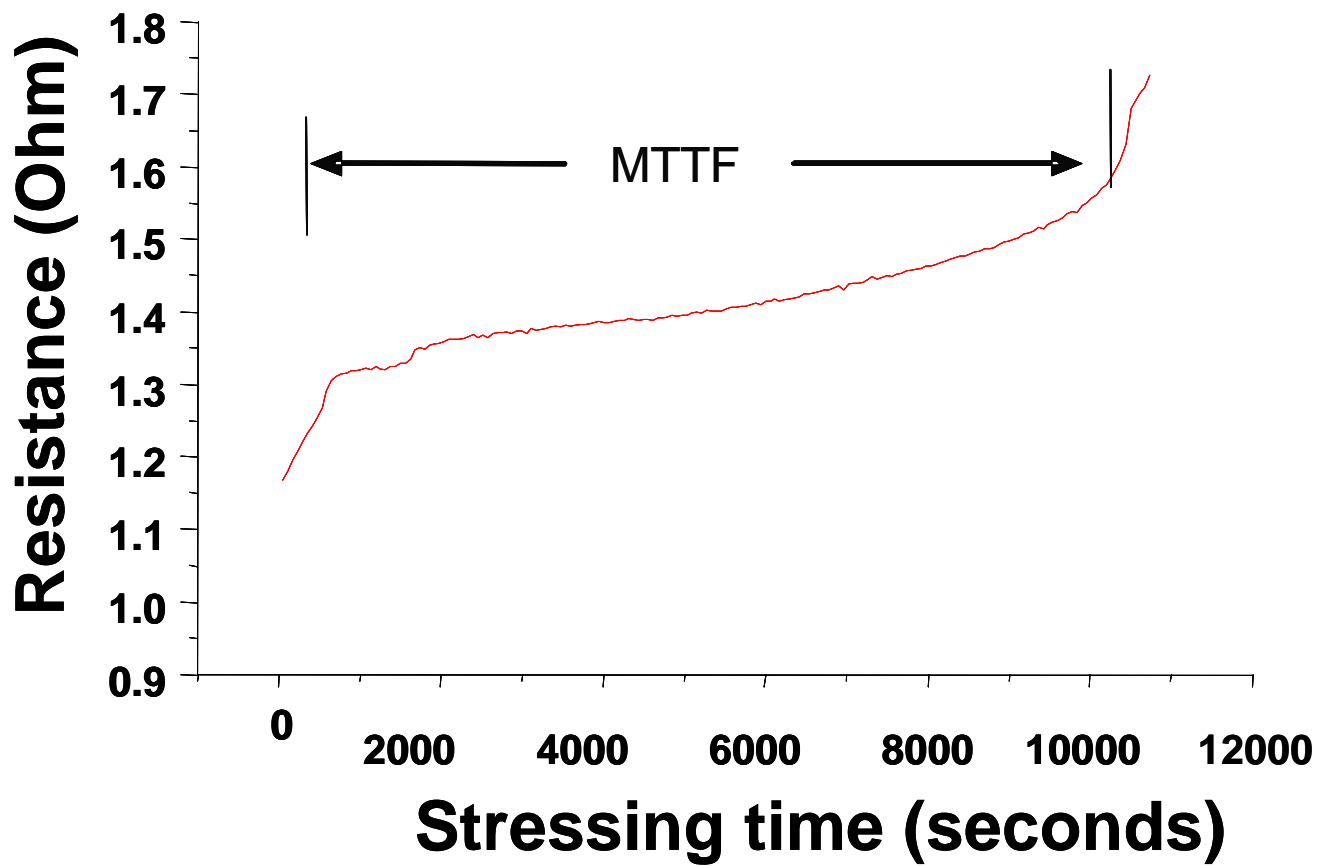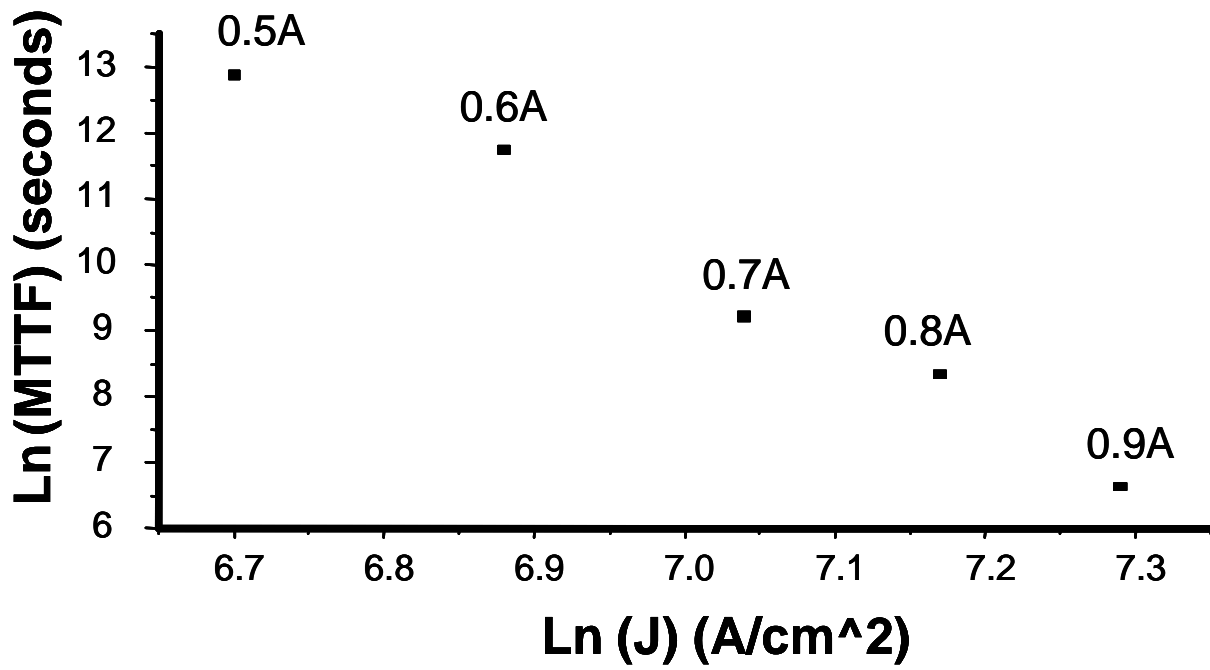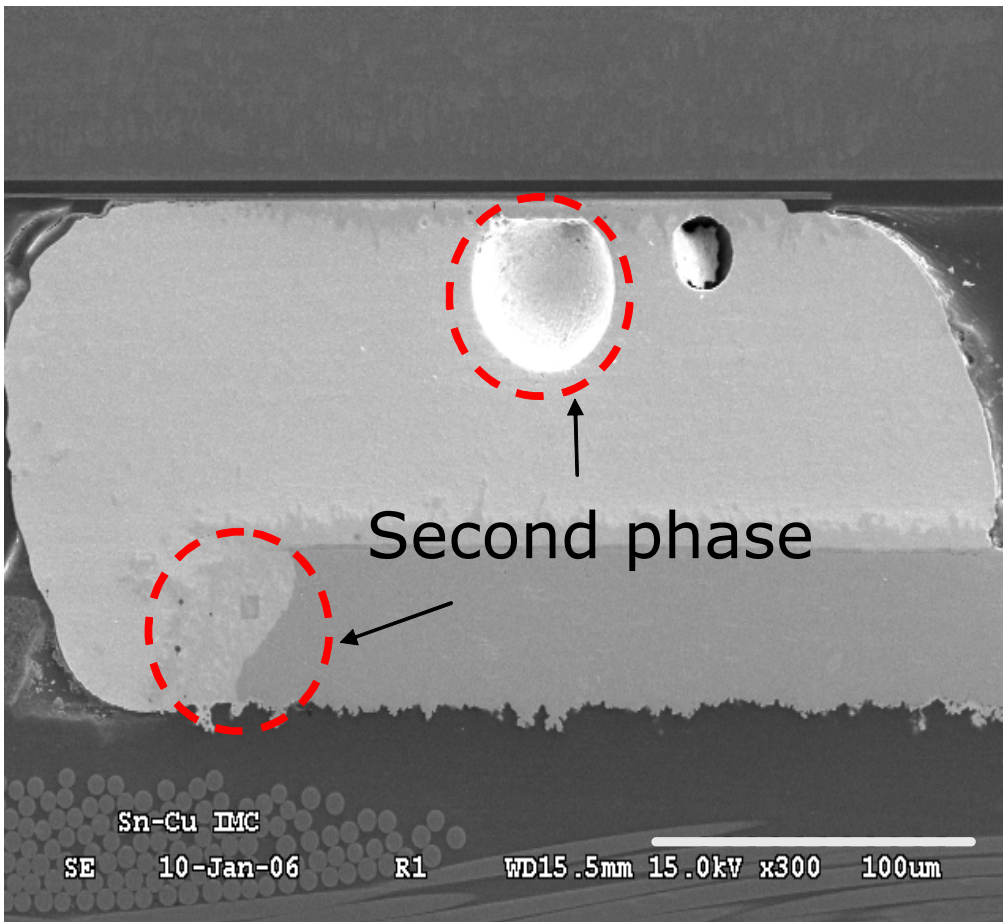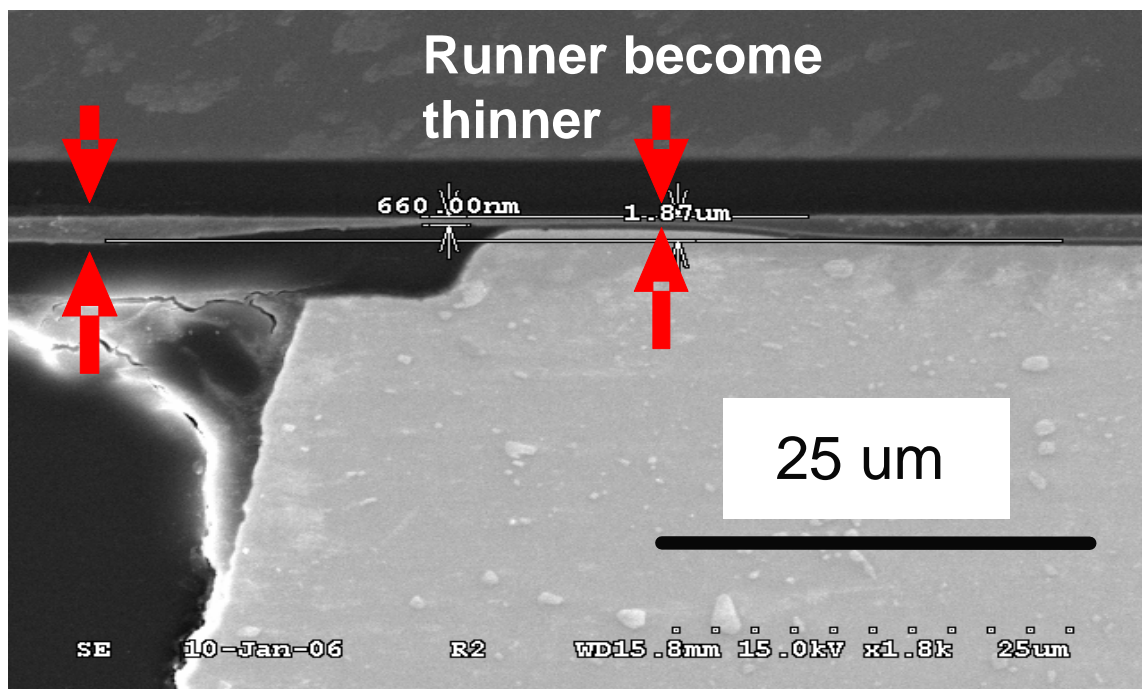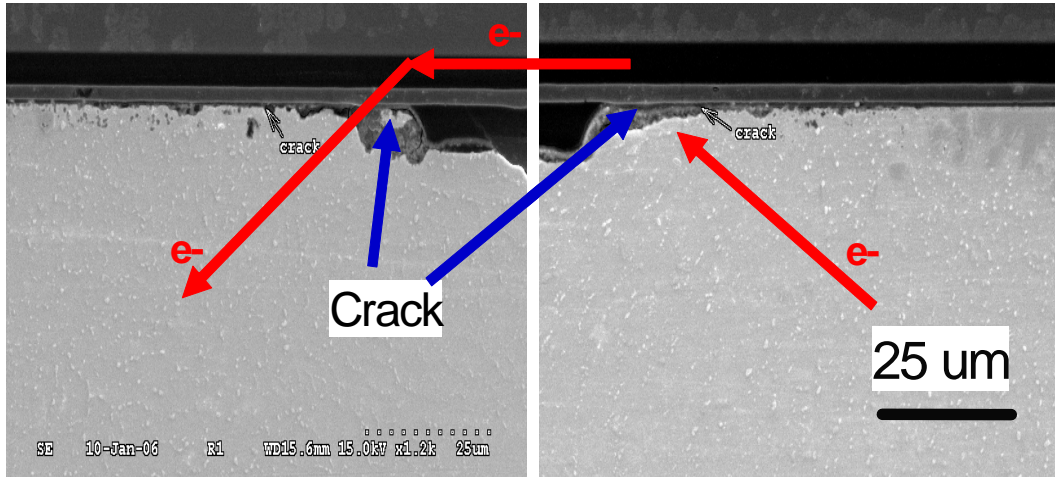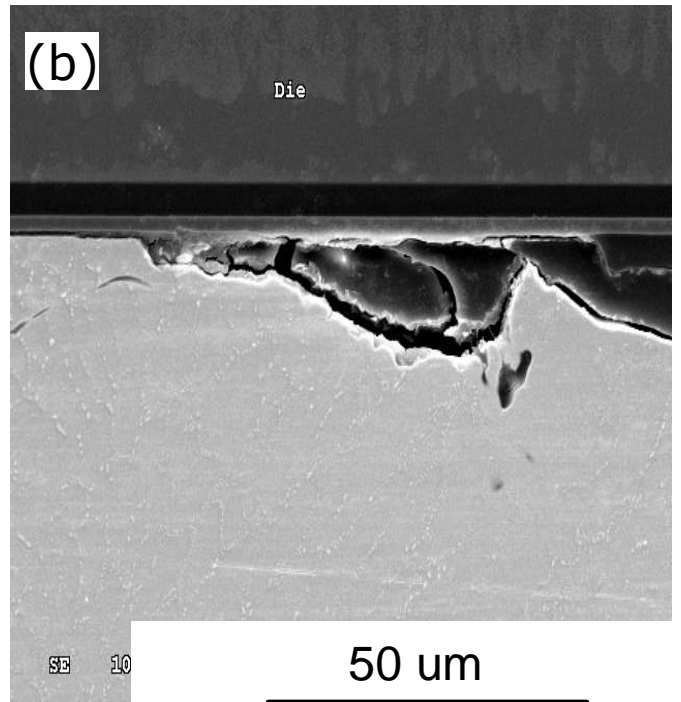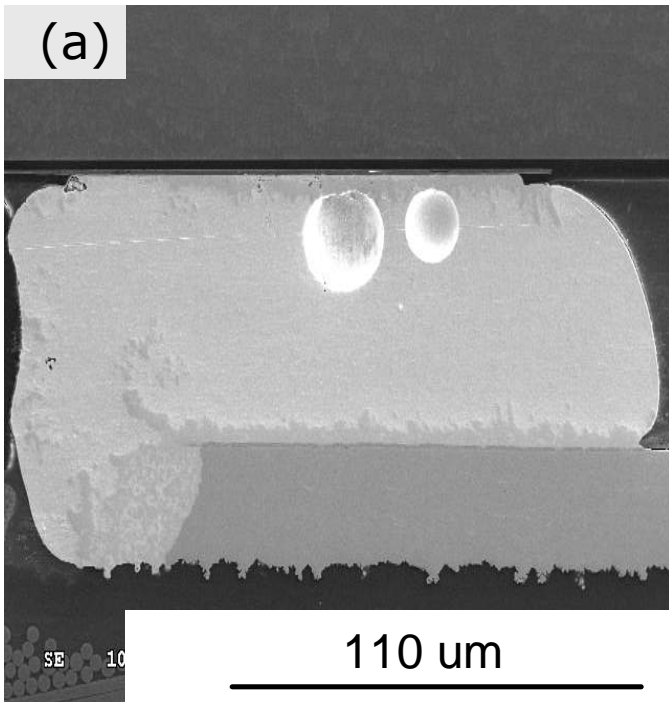
Fig. 9

P. Y. Chen et al

Package Type	WLCSP
Package Dimensions	6.35x6.8
Passivation Type	Polymide
Die Size	6.35x6.8
UBM	4KA Al / 3.25KA NiV / 8KA Cu
UBM opening	280 um
Runner	2KA Ti / 15KA Al / 2KA Ti
Bump Composition	Sn/Ag4.0/Cu0.5
No. of bump	98
Bump pitch	0.5mm
Ball Size	0.3mm
Ball pitch	0.5mm
Surface finishing	Au/Ni
Board thickness	0.8 mm
Pad	NSMD

Table I

P. Y. Chen et al